Specification for Approval

PRODUCT NAME: RGS15128128YR000

PRODUCT NO.: Z J Y 1 5 0 L Y

CUSTOMER
APPROVED BY
DATE:

RITDISPLAY CORP. APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ INITIAL RELEASE	2008. 05. 26	
X02	■ Modify FPC to hot-bar type	2008. 06. 05	Page 16
X03	■ Modify definition of panel thickness ■ Add lifetime specifications ■ Modify D.C electrical characteristics ■ Add panel electrical specifications ■ Add graphic display data ram address map ■ Add interface timing chart ■ Add power on/off sequence ■ Add application circuit	2009. 06. 25	Page 5, 6, 7, 8, 11, 12, 13, 14, 15 & 16
X04	■ Add the information of module weight ■ Modify recipe ■ Modify application circuit ■ Modify seal color (white→black)	2010. 11. 09	Page 5, 6, 8, 16 & 18
A01	■ Transfer from X version ■ Add the packing specification	2011. 11. 21	Page 19
A02	■ Add appendix of precautions for using the OLED module	2014. 03. 31	Page 24~33

CONTENTS

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : Yellow
- Panel resolution : 128*128
- Driver IC : SSD1327
- Excellent Quick response time : 10µs
- Extremely thin thickness for best mechanism design : 1.41 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface, I^2C Interface.
- Wide range of operating temperature : -40 to 70℃
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 x 128	dot
2	Dot Size	0.19 (W) x 0.19 (H)	mm^2
3	Dot Pitch	0.21 (W) x 0.21 (H)	mm^2
4	Aperture Rate	82	%
5	Active Area	26.86 (W) x 26.86 (H)	mm^2
6	Panel Size	33.8 (W) x 36.5 (H)	mm^2
7*	Panel Thickness	1.22 $\pm$ 0.1	mm
8	Module Size	33.8 (W) x 43.7 (H) x 1.41 (T)	mm^3
9	Diagonal A/A size	1.5	inch
10	Module Weight	3.48 $\pm$ 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{CI})	-0.3	4	V	Ta = 25℃	IC maximum rating
Supply Voltage (Vcc)	8	19	V	Ta = 25℃	IC maximum rating
Operating Temp.	-40	70	℃		
Storage Temp	-40	85	℃		
Humidity		85	%		
Life Time	20,000	-	Hrs	120 cd/m², 50% checkerboard	Note (1)
Life Time	24,000	-	Hrs	100 cd/m², 50% checkerboard	Note (2)
Life Time	30,000	-	Hrs	80 cd/m², 50% checkerboard	Note (3)

Note:

    (A) Under Vcc = 15V, Ta = 25℃, 50% RH.

    (B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 120 cd/m² :
- Contrast setting : 0x74
- Frame rate : 105Hz
- Duty setting : 1/128

(2) Setting of 100 cd/m² :
- Contrast setting : 0x60
- Frame rate : 105Hz
- Duty setting : 1/128

(3) Setting of 80 cd/m² :
- Contrast setting : 0x4A
- Frame rate : 105Hz
- Duty setting : 1/128

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{CC}	Driver power supply (for OLED panel)	-		14.5	15	15.5	V
V_{CI}	Low voltage power supply	-		2.6	-	3.5	V
V_{OH}	High logic output level	Iout=100uA,		$0.9* V_{CI}$	-	V_{CI}	V
V_{OL}	Low logic output level	Iout=100uA,		0	-	$0.1* V_{CI}$	V
V_{IH}	High logic input level	Iout=100uA,		$0.8* V_{CI}$	-	V_{CI}	V
V_{IL}	Low logic input level	Iout=100uA,		0	-	$0.2* V_{CI}$	V
I_{CC}	V_{CC} Supply Current	V_{CI} = 3.5V, V_{CC} = 18V, Display ON, No panel attached, contrast = FF	External V_{DD}= 2.5V	600		750	uA
			Internal V_{DD}= 2.5V	600		750	
I_{CI}	V_{CI} Supply Current	V_{CI} = 3.5V, V_{CC} = 18V, Display ON, No panel attached, contrast = FF	External V_{DD}= 2.5V	35		50	uA
			Internal V_{DD}= 2.5V	95		120	
I_{SEG}	Segment output current Setting V_{CC}=18V, IREF=10uA	Contrast=FF		-	300	370	uA
		Contrast=AF		-	206	-	uA
		Contrast=7F		-	150	-	uA
		Contrast=3F		-	75	-	uA
		Contrast=1F		-	37.5	-	uA

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

| PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current consumption	-	15	17	mA	All pixels on
Standby mode current consumption	-	1	2	mA	Standby mode 10% pixels on
Normal mode power consumption	-	225	255	mW	All pixels on
Standby mode power consumption	-	15	30	mW	Standby mode 10% pixels on
Pixel Luminance	80	100		cd/m^2	Display Average
Standby Luminance		25		cd/m^2	
CIEx (Yellow)	0.43	0.47	0.51		CIE1931
CIEy (Yellow)	0.48	0.52	0.56		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		µs	

Normal mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x60
- Frame rate : 105Hz
- Duty setting : 1/128

Standby mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x00
- Frame rate : 105Hz
- Duty setting : 1/128

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM
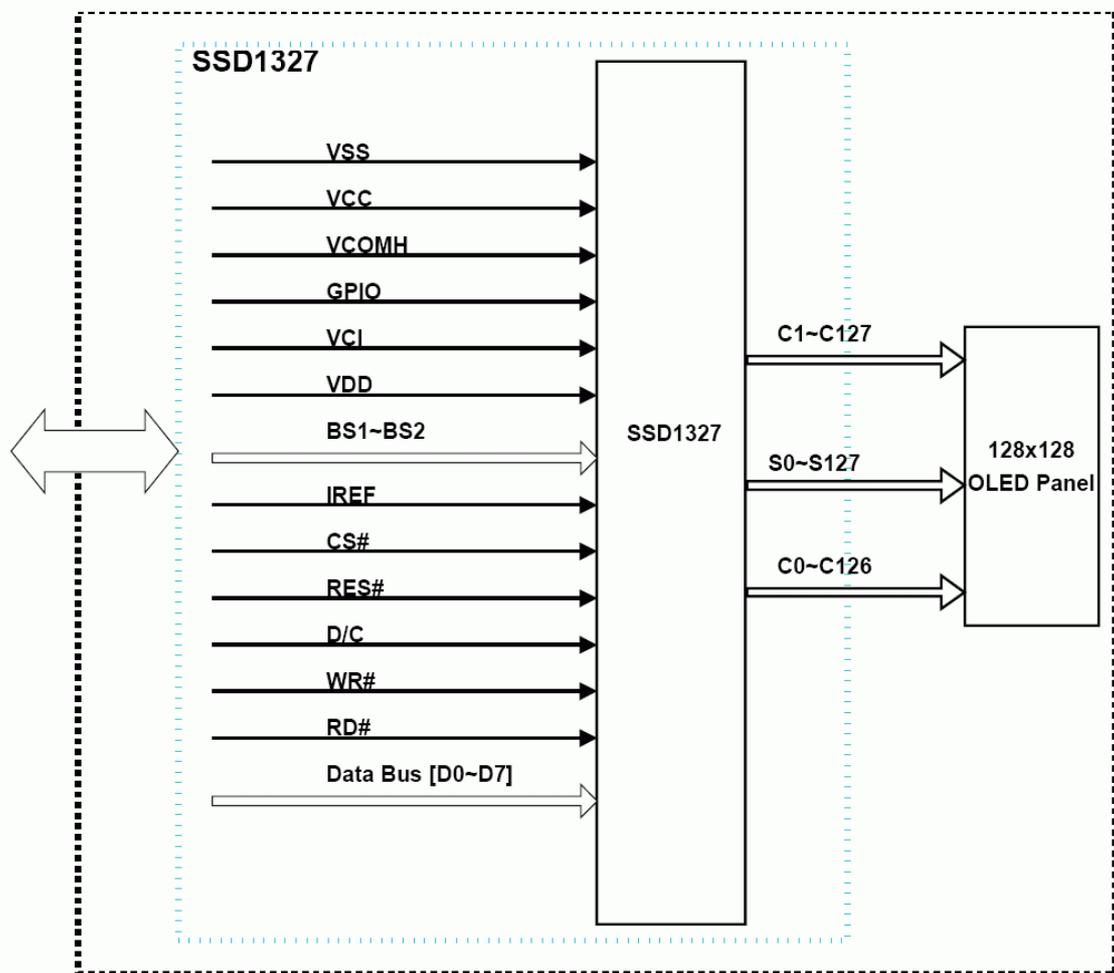
RiTdisplay 128X128 OLED Module

7.2 PANEL LAYOUT DIAGRAM

SEG & COM Layout
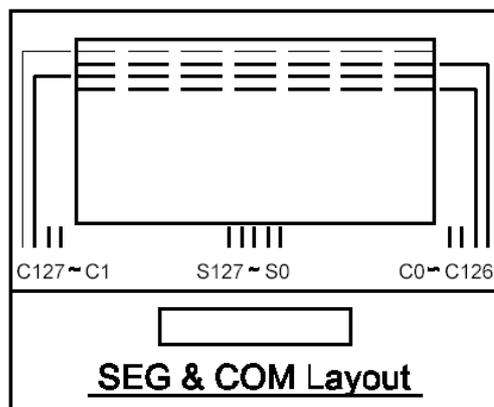
7.3 PIN ASSIGNMENTS

Pin No.	Pin Name	Description
1	VSS	Ground.
2	VCC	Power supply for analog circuit.
3	VCOMH	Com Voltage Output. A capacitor should be connected between this pin and V_{SS}.
4	GPIO	General I/O port.
5	VCI	Power supply for logic circuit.
6	VDD	A capacitor should be connected between this pin and V_{SS}.
7	BS1	MCU bus interface selection pins.
8	BS2	MCU bus interface selection pins.
9	VSS	Ground.
10	IREF	Reference current input pin. A resistor should be connected between this pin and V_{SS}.
11	CS#	Chip select input.
12	RES#	Reset signal input. When it's low, initialization of SSD1327 is executed.
13	D/C	Data / Command control. Pull high for write/read display data. Pull low for write command or read status.
14	WR#	MCU interface input. Data write operation is initiated when it's pull low.
15	RD#	MCU interface input. Data read operation is initiated when it's pull low.
16	D0	Data bus(for parallel interface)
17	D1	
18	D2	
19	D3	
20	D4	
21	D5	
22	D6	
23	D7	
24	VCC	Power supply for analog circuit.
25	VSS	Ground.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps below tables show some examples on using the command "Set Re-map" A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 … D8189, D8190, D8191 represent the 128x128 data bytes in the GDDRAM.

The GDDRAM map under the following condition:
● Command "Set Re-map" A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Horizontal Address Increment (A[2]=0)
  Disable COM Re-map (A[4]=0)
● Display Start Line=00h
● Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 1

The GDDRAM map under the following condition:
- Command "Set Re-map" A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Vertical Address Increment (A[2]=1)
  Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 2

COM Outputs	Row Address (HEX)	SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address (HEX)
COM0	00	D0[3:0]	D0[7:4]	D128[3:0]	D128[7:4]		D7936[3:0]	D7936[7:4]	D8064[3:0]	D8064[7:4]	
COM1	01	D1[3:0]	D1[7:4]	D129[3:0]	D129[7:4]		D7937[3:0]	D7937[7:4]	D8065[3:0]	D8065[7:4]	
COM126	7E	D126[3:0]	D126[7:4]	D254[3:0]	D254[7:4]		D8062[3:0]	D8062[7:4]	D8190[3:0]	D8190[7:4]	
COM127	7F	D127[3:0]	D127[7:4]	D255[3:0]	D255[7:4]		D8063[3:0]	D8063[7:4]	D8191[3:0]	D8191[7:4]	

(Display Startline=0)

Nibble re-map A[1]=0

The GDDRAM map under the following condition:
- Command "Set Re-map" A0h is set to:
  Enable Column Address Re-map (A[0]=1)
  Enable Nibble Re-map (A[1]=1)
  Enable Horizontal Address Increment (A[2]=0)
  Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

GDDRAM address map 3

COM Outputs	Row Address (HEX)	SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		3F		3E			01		00		Column Address (HEX)
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]	
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]	
COM126	7E	D8127[7:4]	D8127[3:0]	D8126[7:4]	D8126[3:0]		D8065[7:4]	D8065[3:0]	D8064[7:4]	D8064[3:0]	
COM127	7F	D8191[7:4]	D8191[3:0]	D8190[7:4]	D8190[3:0]		D8129[7:4]	D8129[3:0]	D8128[7:4]	D8128[3:0]	

(Display Startline=0)

Nibble re-map A[1]=1

REV.: A02   2014/03/31
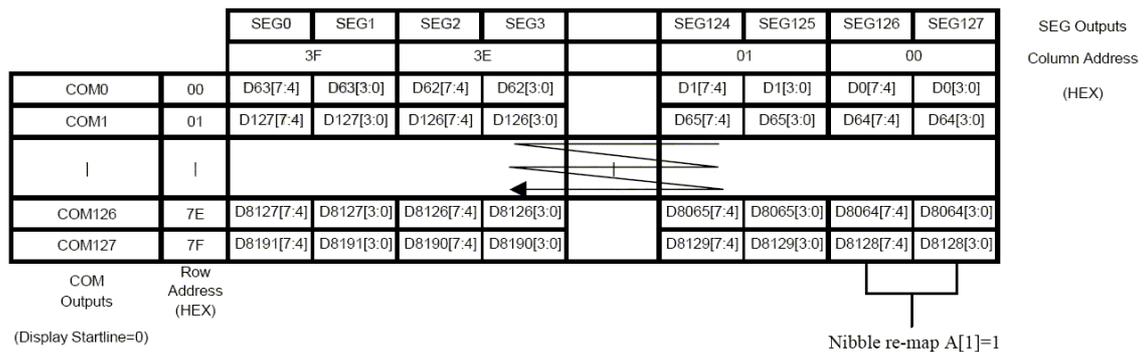
The example in which the display start line register is set to 10h with the following condition:

- Command "Set Re-map" A0h is set to:
    Disable Column Address Re-map (A[0]=0)
    Disable Nibble Re-map (A[1]=0)
    Enable Horizontal Address Increment (A[2]=0)
    Enable COM Re-map (A[4]=1)
- Display Start Line=78h (corresponds to COM119)
- Data byte sequence: D0, D1, D2 … D8191
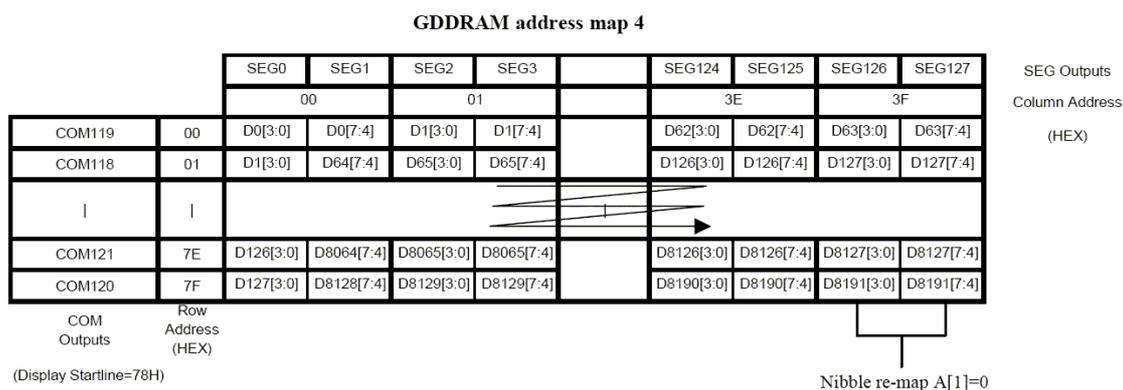
GDDRAM address map 4

COM Outputs	Row Address (HEX)	SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address (HEX)
COM119	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM118	01	D1[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
|	|										
COM121	7E	D126[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]	
COM120	7F	D127[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]	

(Display Startline=78H)

Nibble re-map A[1]=0

The GDDRAM map under the following condition:
- Command "Set Re-map" A0h is set to:
    Disable Column Address Re-map (A[0]=0)
    Disable Nibble Re-map (A[1]=0)
    Enable Horizontal Address Increment (A[2]=0)
    Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=7Eh
- Data byte sequence: D0, D1, D2 … D7811

GDDRAM address map 5

COM Outputs	Row Address (HEX)	SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address (HEX)
COM0	00										
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]			
|	|										
COM126	7E			D7750[3:0]	D7750[7:4]		D7811[3:0]	D7811[7:4]			
COM127	7F										

(Display Startline=0)

Nibble re-map A[1]=0
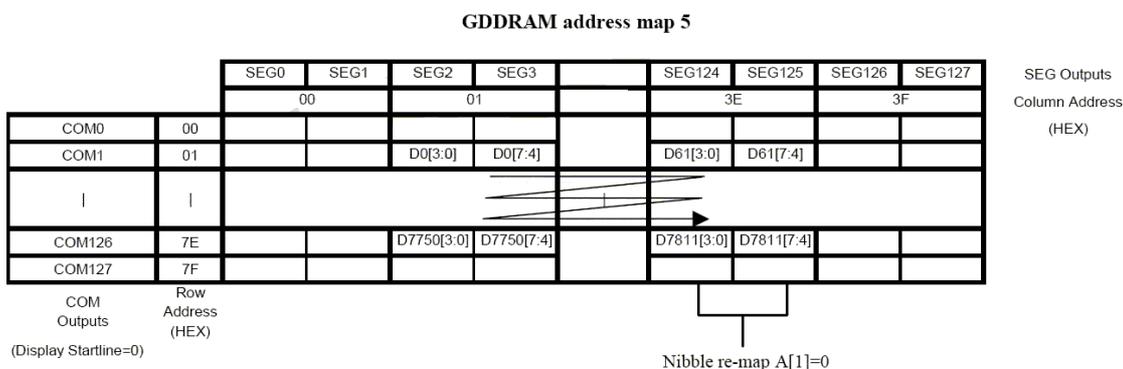
7.5 INTERFACE TIMING CHART

8080-Series MCU Parallel Interface Timing Characteristics

$(V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{CI} = 3.3V$, $T_A = 25°C)$

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

**8080-series MCU parallel interface characteristics**
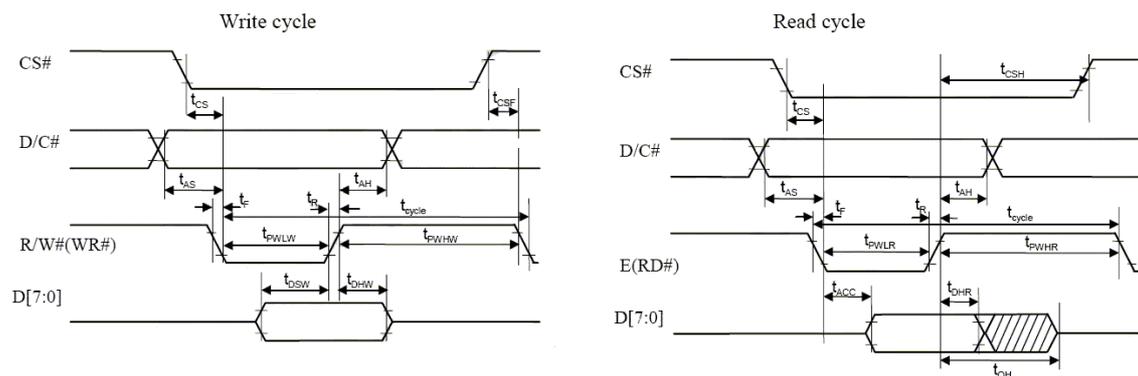
8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

Power ON sequence:

1. Power ON V_{CI}.
2. After V_{CI} becomes stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

The Power ON sequence.
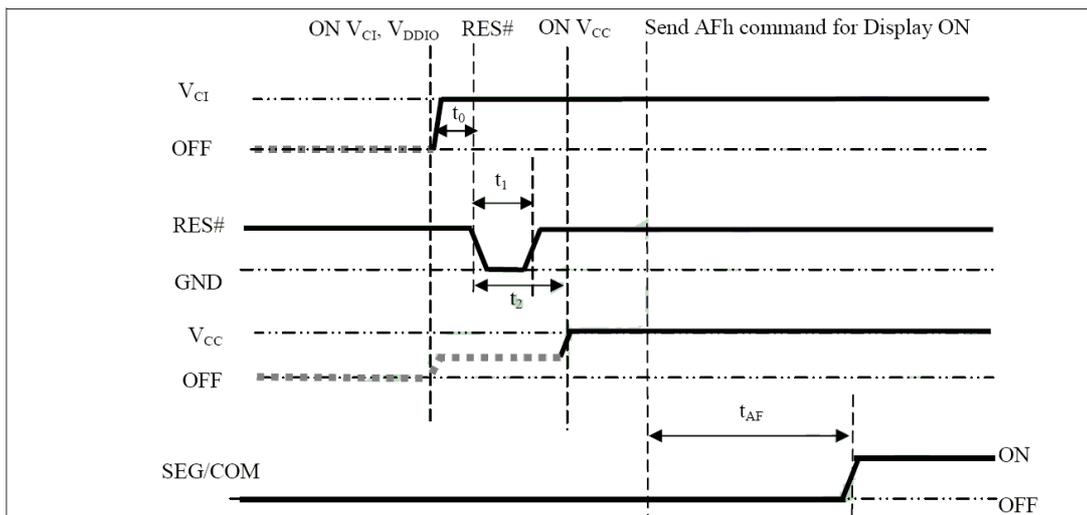
Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2], [3]
3. Wait for t_{OFF}. Power OFF V_{CI}.(where Minimum t_{OFF}=80ms [5], Typical t_{OFF}=100ms)

The Power OFF sequence
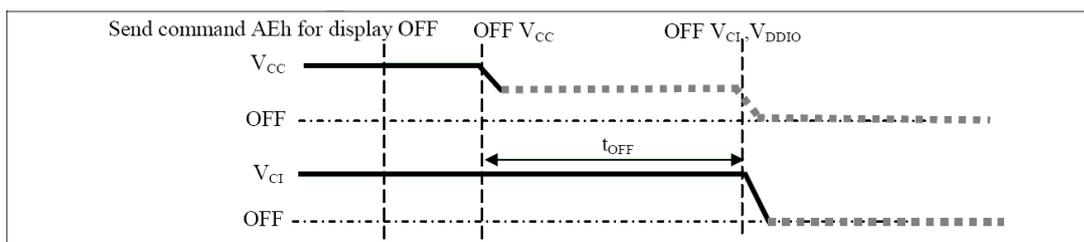
Note:

(1) Since an ESD protection circuit is connected between V_{CI} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be kept disable when it is OFF.

(3) Power pins (V_{CI}, V_{CC}) can never be pulled to ground under any circumstance.

(4) The register values are reset after t_1.

(5) V_{CI} should not be Power OFF before V_{CC} Power OFF

REV.: A02   2014/03/31

8.2 APPLICATION CIRCUIT
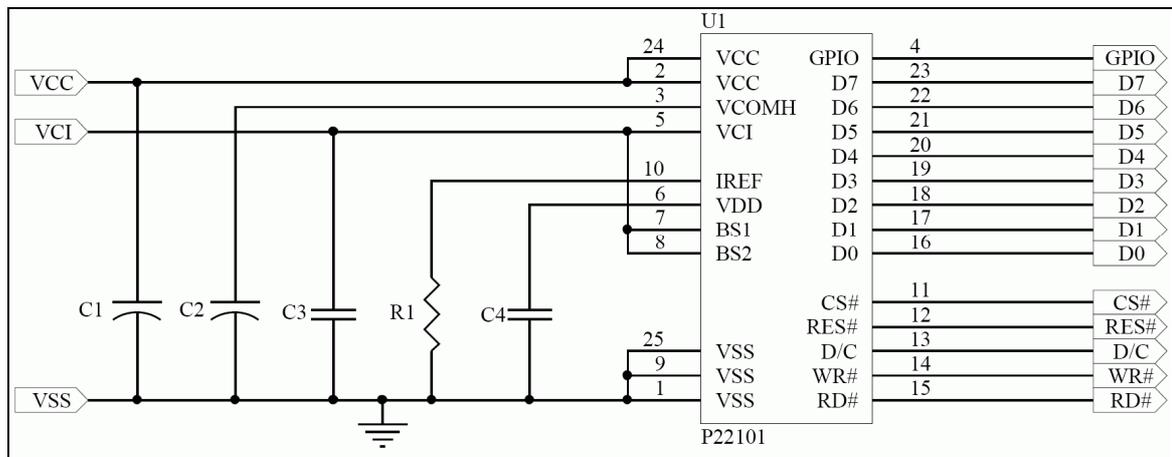
Component:

    C1, C2: 4.7uF/35V(Tantalum type) or VISHAY (572D475X0025A2T)

    C3, C4: 1uF/16V(0603)

    R1: 2M ohm (0603) 1%

This circuit is for 8080 8bits interface.

8.3 COMMAND TABLE

Refer to IC Spec.: SSD1327

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85℃, 240hrs	5
2	High temp. (Operation)	70℃, 120hrs	5
3	Low temp. (Operation)	-40℃, 120hrs	5
4	High temp. / High humidity (Operation)	65℃, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40℃ ~85℃ (-40℃ /30min; transit /3min; 85℃ /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

Test and measurement conditions
1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria
1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION

Revision	Date	Note
03	2010/10/06	Modify seal

Pin Assignment

NO.	SYMBOL
1	VSS
2	VCC
3	VCOMH
4	GPIO
5	VCI
6	VDD
7	BS1
8	BS2
9	VSS
10	IREF
11	CS#
12	RES#
13	D/C
14	WR#
15	RD#
16	D0
17	D1
18	D2
19	D3
20	D4
21	D5
22	D6
23	D7
24	VCC
25	VSS

SEG & COM Layout

C0~C126
S127~S0
C127~C1

Specification
1.Display: OLED(Yellow)
2.Dot Matrix: 128x128
3.Dot Size: 0.19x0.19mm
4.Dot Pitch: 0.21x0.21mm
5.Aperture Rate: 82%
6.Active Area: 26.86x26.86mm
7.IC: SSD1327Z

128x128 Dots(1.5")

33.8±0.2
32.8±0.3 (AG Polarizer)
28.86 (V/A)
P0.21x128-0.02=26.86(A/A)

P0.21x128-0.02=26.86(A/A)
28.86 (V/A)
29.8±0.3(Polarizer)
30.8±0.2 (Cover Glass)
36.5±0.2
(43.7)

(0.5)
(2.47)
(3.47)
(5)
0.7
1.41±0.1 (w/o two Handlers)
Handlers 15x5x0.15mm
AG Polarizer t=0.19mm
5.7 Max.
1.5 Max.
Symbio,Inc. PO6B (Silver) 16x4x0.07mm
Contact Side Plating:Ni-Au
Contact Side Plating:Ni-Au
(Seal Cover IC:Black)
(Seal,Black)

0.02
0.19
0.21
0.19
0.21
0.02

8.4±0.3
(1.2)
2-□0.8±0.1
Φ0.2(PTH)
1.65±0.1
(7.95)
R0.225
25
10±0.2
(0.5)
W=0.35±0.03
P0.65x(25-1)=15.6±0.05
17.5±0.1(Alignment hole)
18.9±0.3
0.5±0.3
0.6±0.1
2±0.3
3.2±0.2
Pin 1
(3.9)
(6.95)
(1.9)
(0.9)
(0.5)
(7.2)

General Tolerance

Length (mm)	Tolerance(mm)
0 ~ 8	±0.1
8 ~ 25	±0.2
25 ~ 50	±0.3

	CONFIDENTIAL	Scale	Unit	Sheet	PROJECT CODE	P22101
	Third Angle Projection	2.5:1	mm	1/1	PART NAME	Module Ass'y
M.E.	E.E.	Module	Spec.	Approved	PARTS NO.	9822101000
Valerie Lo	Kevan Huang	Valerie Lo	Irene Fan	Strong Tsai	REVISION	03
					REVISION	03

RITEK GROUP RiTdisplay Corporation

11. PACKING SPECIFICATION

Revision	Date	Note
01	2011/11/21	Packing Tray Instruction

④ 3003000012
Vacuum Bag ONY/LDPE
真空包裝袋 ONY/LDPE
480x285x90
Vacuum packing : 4 sec
抽真空:4 秒

③ 3010000003
5G Silica Gel Desiccants
5G 乾燥劑
x4 pcs

⑤ 3003000016
Antistatic Bubble bag 440x(350+450)mm
抗靜電氣泡袋

Tray =21 pcs

⑨ Tape 膠帶 3208000125

⑥ 3001000005
Pizza Box 345x285x88,B corrugated
B 浪

x2 pcs

Label 標籤
⑧ 3006000000
Label x2 pcs

⑦ 3000000009
Carton 385x305x203mm

Label 標籤
⑧ 3006000000
Label x1 pcs

⑨ Tape 膠帶 3208000125

9822101000
Module Ass'y For P22101 x30 pcs
①
Face up , Rotate packing
面朝上,旋轉放置

3008000362 ②
Tray 330x270x8.7mm　T=0.7mm,PS,P22102

x 1 pcs(empty)
x 20 pcs
Rotate stack 旋轉堆疊

ITEM	PART No.	DESC	QTY
	9922101000	Module Ass'y For P22101	1
1	9822101000	Module Ass'y For P22101	1200
2	3008000362	Tray 330x270x8.7 T:0.7mm PS P22102	42
3	3010000003	5G Silica Gel Desiccants	8
4	3003000012	Vacuum Bag ONY/LDPE 480x285x90	2
5	3003000016	Antistatic Bubble bag 440x(350+450)mm	2
6	3001000005	Pizza Box 345x285x88,B corrugated	2
7	3000000009	Carton 385x305x203mm	1
8	3006000000	Label	3
9	3208000125	Tape, W=48mm , L=910cm	

RITEK GROUP
RiTdisplay Corporation

PROJECT CODE		P22101		VERSION	01
PART NAME		Packing Tray Instruction		VERSION	01
PARTS NO.		9922101000			

Sheet	1/1	Approved	Strong Tsai
Scale	1:15	Module	Kelly Hsu
Unit	mm	Spec.	Irene Fan

General Tolerance		CONFIDENTIAL	Third Angle Projection	
Length (mm)	Tolerance(mm)	M.E.	E.E.	
0 ~ 8	±0.1	Iven Lee		
8 ~ 25	±0.2			
25 ~ 50	±0.3			

12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.
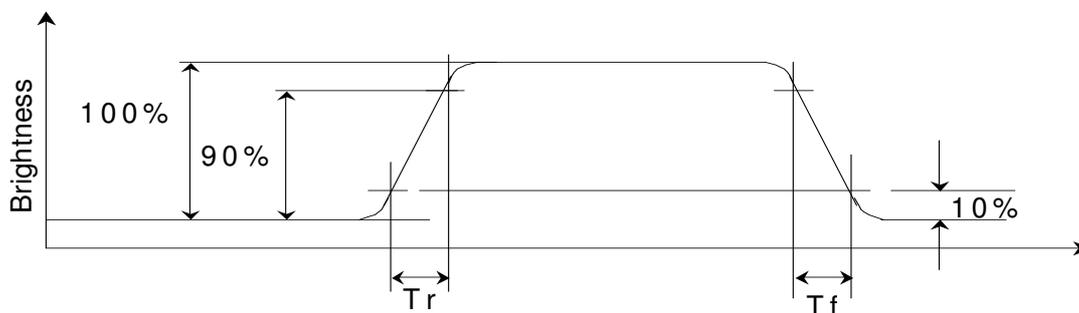
Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.
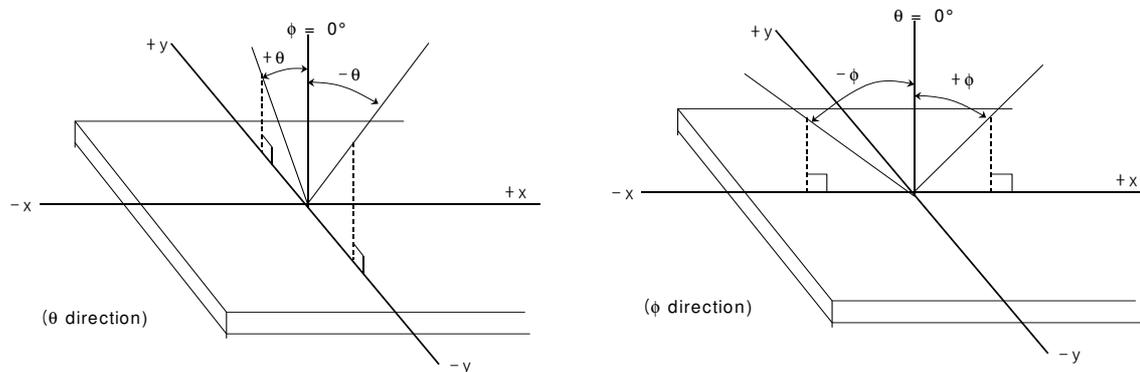
Figure 3 Viewing angle

REV.: A02   2014/03/31

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

Measurement
Header

Panel

Plate Form

PR-705 /
MINOLTA CS-100
Color Analyzer
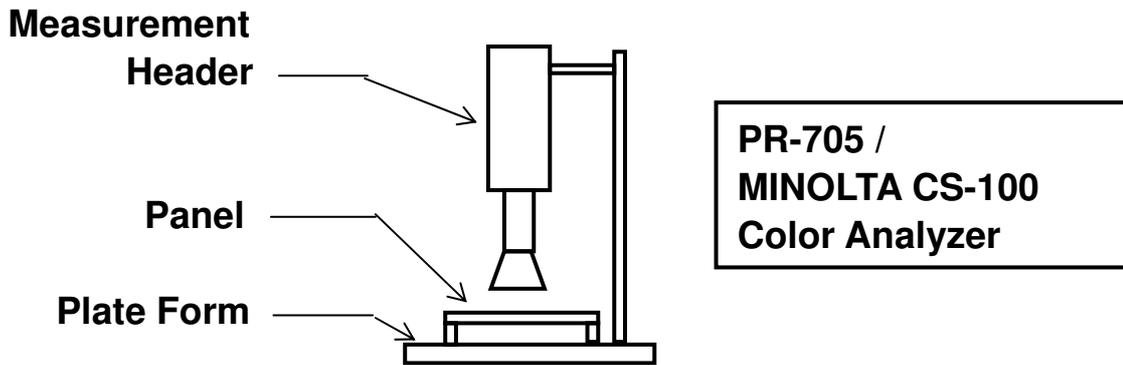
B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510

Measurement
Header

Panel

Plate Form

Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer

REV.: A02   2014/03/31
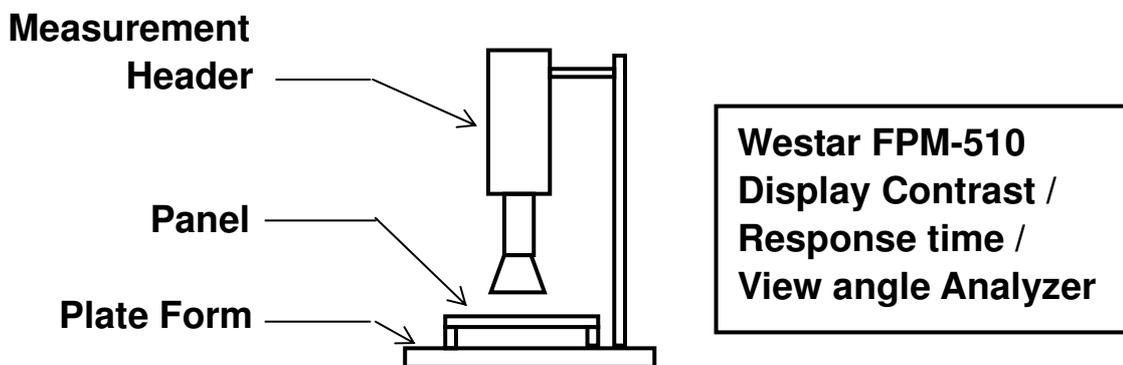
C. ESD ON AIR DISCHARGE MODE

REV.: A02   2014/03/31
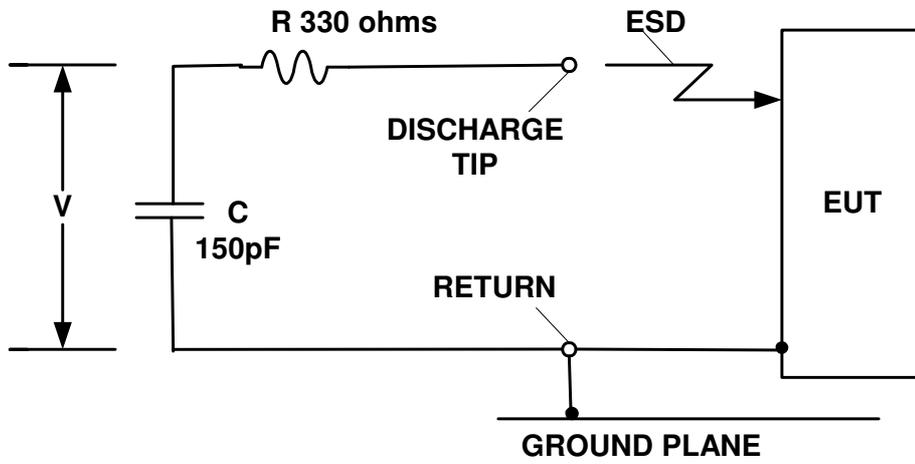
APPENDIX 3: PRECAUTIONS FOR USING THE OLED MODULE

Precautions for Handling

1. When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.

2. The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a high position.

3. The OLED module is an electronic component and is subject to damage caused by Electro Static Discharge (ESD). And hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Also, ground the tools being used for panel assembly and make sure the working environment is not too dry to cause ESD problems. Antistatic wrist strap should touch human body directly instead of gloves. (See below photos).
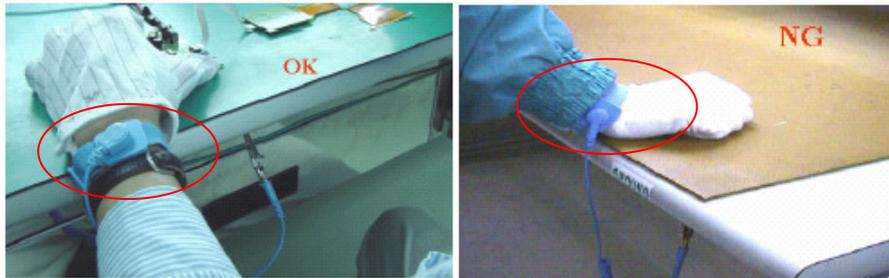
4. Take out the panel one by one from the holding trays for assembly, and never put the panel on top of another one to avoid the scratch.

5. Avoid jerk and excessive bend on TAB/FPC/COF, and be careful not to let foreign matter or bezel damage the film.

6. When handling and assembling the module (panel + IC), grab the panel, not the TAB/FPC/COF.

7. Use the tweezers to open the clicks on the connector of PCB before the insertion of FPC/COF, and click them back in. Once the FPC/COF sits properly in the connector, use the tweezers to avoid the damages.

- 24 -   REV.: A02   2014/03/31

8. Please do not bend the film near the substrate glass. It could cause film peeling and TAB/FPC/COF damage. For TAB, It should bend the slit area as actual OLED it is. For FPC or COF, it is suggested to follow below pictures for instruction (distance between substrate glass and bending area >1.5mm; R>0.5mm).

TAB

TAB

FPC

COF

REV.: A02   2014/03/31
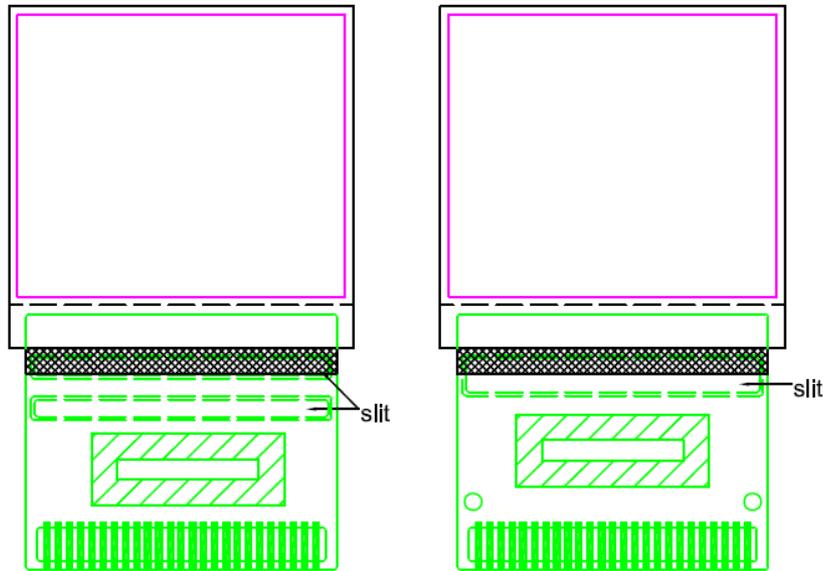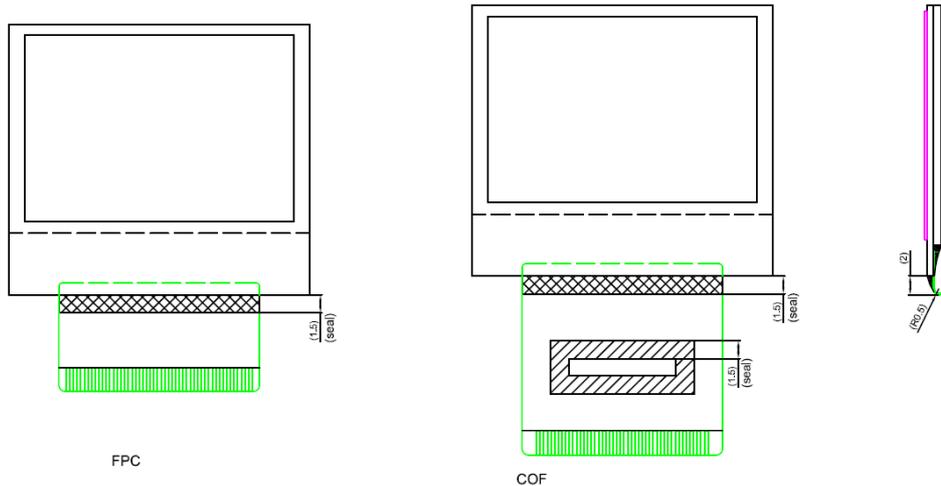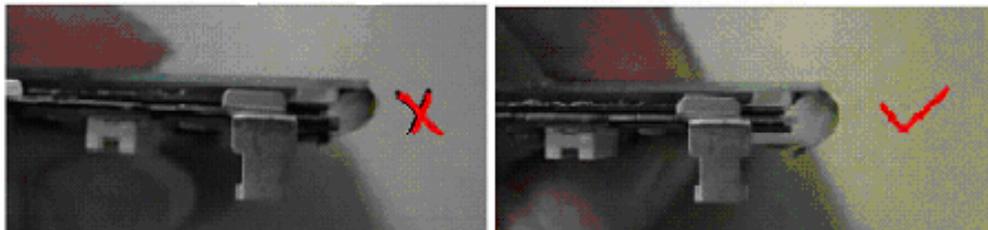
9. Avoid bending the film at IC bonding area. It could damage the IC ILB bonding. It should avoid bending the IC seal area. Please keep the bending distance >1.5mm.

COF
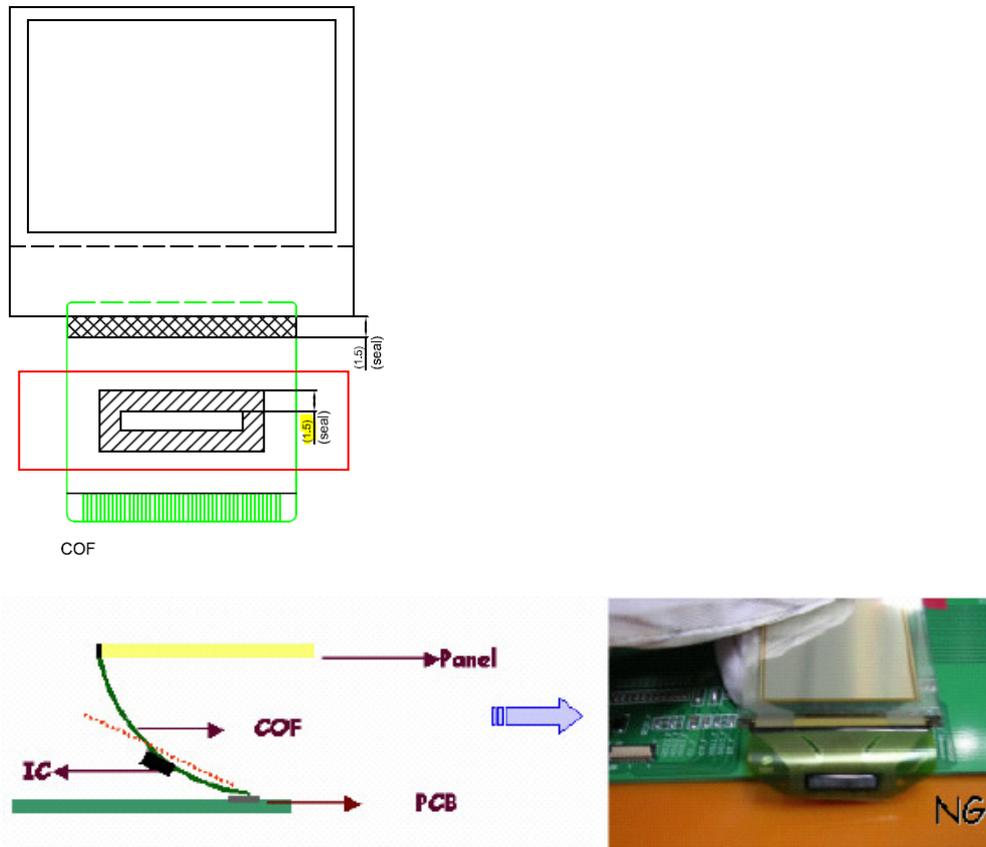
10. Use both thumbs to insert COF into the connector when assembling the panel. Please refer to the photo.
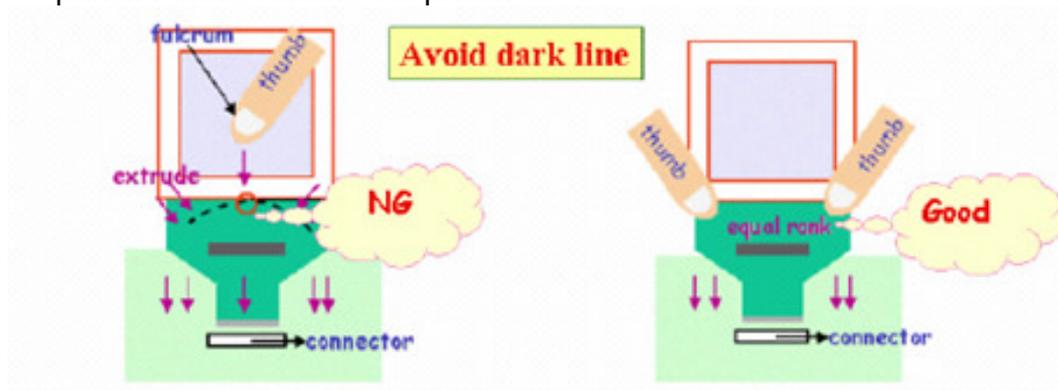
11. The working area for the panel should be kept clean. If the panel is accidentally dropped on the floor, do visual inspection of the panel first. Please use clean-room wiping cloth moistened with alcohol to wipe it off if dirt or grease stains the panel.

12. Do not wipe the pin of film and polarizer with the dry or hard materials that will damage the surface. When cleaning the display surface, use the soft cloth with solvent, IPA or alcohol, to clean.

13. Protection film is applied to the surface of OLED panel to avoid the scratch. Please remove the protective film before assembling it. If the OLED panel has been stored for a long time, the residue adhesive material of the protective film may remain on the display surface after remove the protective film. Please use the soft cloth with solvent, IPA or alcohol, to clean.

14. When hand or hot-bar soldering TAB/FPC onto PCB, make sure the temperature and timing profiles to meet the requirements of soldering specification (the specification depends on the application or optimized by customer) to prevent the damage of IC pins by inappropriate soldering.

15. Solder residues arise from soldering process have to be cleaned up thoroughly before the module assembly.

16. Use the voltage and current settings listed in the specification to do the function test after the module assembly.

17. Suggestion for soldering process:
   i. TAB Lead- free soldering hot bar process
      1. Use pulse heated bonding tool equipment
      2. Material: Sn/Ag/Cu lead-free solder paste with typical 25um thickness on PCB pad. The TAB pin size and shape may be different, please base on the production line to adjust the thickness of PCB pad and temperature.
      3. Bonding Force:--4kg per centimeter square as the starting point.
      4. Suggested bonding tool temperature & time profile is as below for reference. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.

REV.: A02   2014/03/31
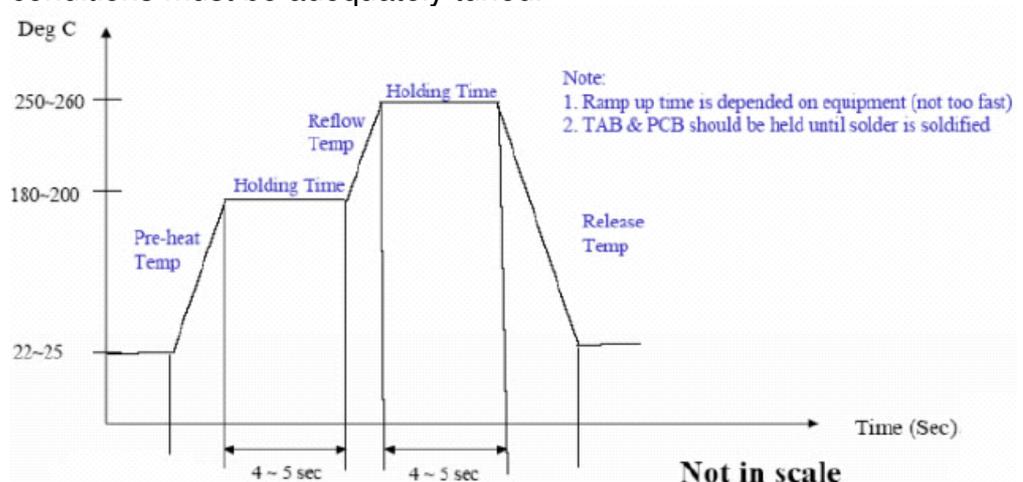
　　ii. TAB Lead- free soldering wire process
　　　　In case of manual soldering (Lead- free solder wire)
　　　1. Solder wire contact iron directly: 280±5℃ at 3-5secs
　　　2. Solder wire contact TAB lead directly (near iron but not contact): 380±5 ℃, 3-5secs
　　　3. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.
　iii. High temperature will result in rapid heat conduction to IC and might cause damage to IC, so please keep the temperature below 380 ℃. Also, avoid damaging the polyimide and solder resist which might take place at high temperatures. Refold cycles base on the de-soldering status, if the plating of pin was damaged, it can not be used again.

　　　　REV.: A02　　2014/03/31

Precautions for Electrical

## 1. Design using the settings in the specification

It is very important to design and operate the panel using the settings listed in the specification. It includes voltage, current, frame rate and duty cycle... etc. Operation the OLED outside the range of the specification should be entirely avoided to ensure proper operation of the OLED.

2. Maximum Ratings

To ensure the proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

3. Power on/off procedure

To avoid any inadvertent effects resulting from inappropriate power on/off operations, please follow the directions of power on/off procedure on page 6. Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, would cause OLED panel malfunction.

Display turn on sequence

DC-DC power off (VCC turn off) → VDD power on → Hardware RESET RESET time depends on driver IC datasheet → Display off → Driver IC initial → DC-DC power on (VCC turn on) → Wait 100ms for VCC stable → Display on → Display start and end address setting → Send display data

Display turn off sequence

Send display off command → DC-DC power off (VCC turn off) → Wait 100ms for VCC reach 0V → VDD power turn off

4. Power savings

 To save power consumption of the OLED, please use partial display or sleep mode when the panel is not fully activated. Also, if possible, make the black background to save power.

 The OLED is a self-luminous device and a particular pixel cluster or image can be lit on via software control. So power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode. The power consumption is almost in directly proportion to the brightness of the panel, and also in directly proportion to the number of pixels lit on the panel. The customer can save the power by the use of black background and sleeping mode. One benefit from using these design schemes is the extension of the OLED lifetime.
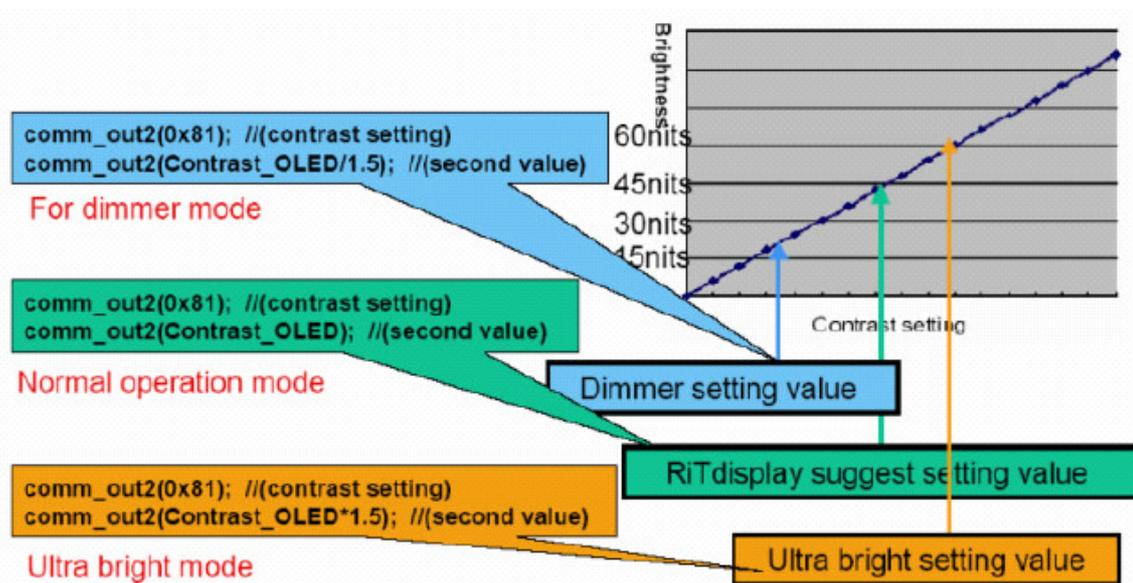
5. Adjusting the luminance of the panel

 Although there are a couple of ways to adjust the luminance of the panel, it is strongly recommended that the customer change the contrast setting to adjust the luminance of the panel. Adjusting voltages to achieve desired luminance is not allowed. Be aware that the adjustment of luminance would accompany the change of lifetime of the panel and its power consumption as well.

6. Residual Image (Image Sticking)

 The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. Image sticking depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following three strategies to minimize image sticking.

1. <u>Employ image scrolling or animation</u> to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.
2. <u>Minimize the use of all-pixels-on or full white background</u> in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays
3. If a static logo is used in the reliability test, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns.

Black Background
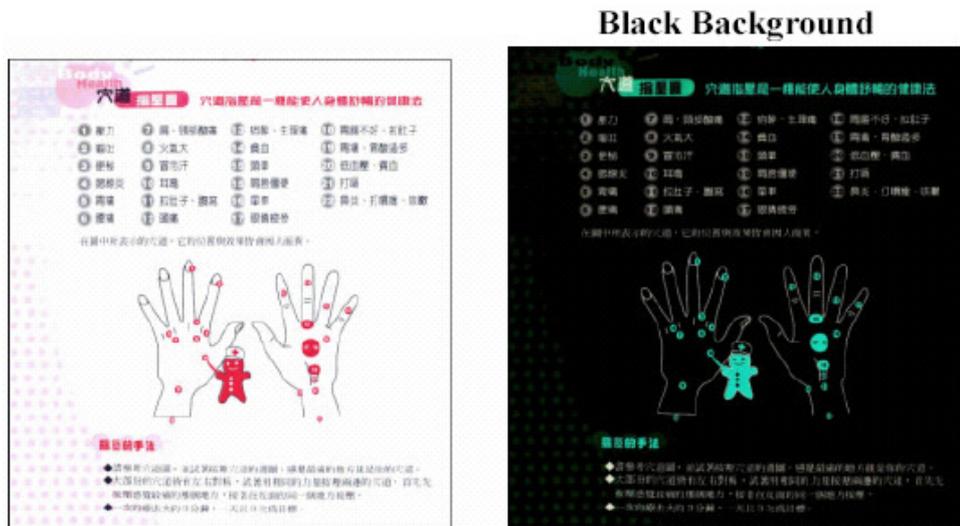
Scrolling example

Frame1

Frame2

Frame3

Frame4

Frame5

Example: setup and start

```
comm_out2(0x26); // scrolling setup
comm_out2(0x08); // scrolling numbers/step
comm_out2(0x00); // start page
comm_out2(0x00); // scrolling step/frame
comm_out2(0x08); // end page
comm_out2(0x2F); // start
```

Example: stop

```
comm_out2(0x2E); //stop
```

REV.: A02   2014/03/31

Precautions for Mechanical

1. Cushion or Buffer tape on the cover glass

It is strongly recommended to have a cushion or buffer tape to apply on the panel backside and front side when assembling OLED panel into module to protect it from damage due to excessive extraneous forces.
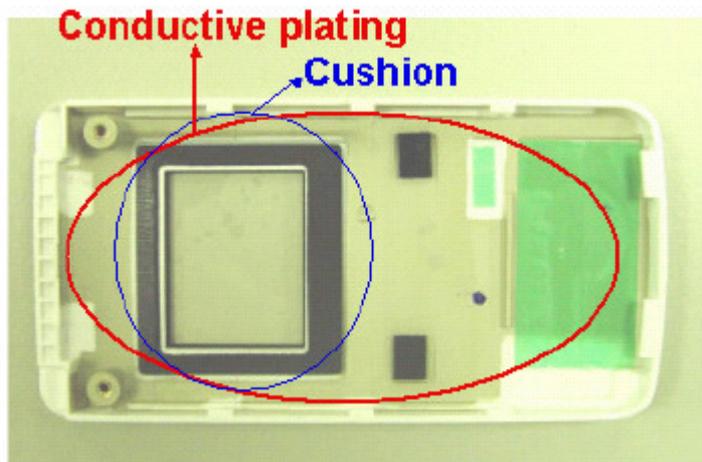
It is recommended that a plating conductive layer be used in the housing for EMI/EMC protection. And, the enough space should be reserved for the IC placement if the IC thickness is thicker than the TAB film when customer design the PCB.

2. Avoid excessive bending of film when handling or designing the panel into the product

The bending of TAB/COF/FPC has to follow the precautions indicated in the specification, extra bending or excessive extraneous forces should be avoided to minimize the chances of film damage. If bending the film is necessary, please bend the designated bending area only. Please refer to items 8 and 9 of Precautions for Handling for more information.

REV.: A02   2014/03/31

Precautions for Storage and Reliability Test

1. Storage

Store the packed cartons or packages at 25℃±5℃, 55%±10%RH. Do not store the OLED module under direct sunlight or UV light. For best panel performance, unpack the cartons and start the production of the panels within six months after the reception of them.

2. Reliability Test

RiTdisplay only guarantees the reliability of the OLEDs under the test conditions and durations listed in the specification.

REV.: A02   2014/03/31